REMARKS

In accordance with section 1215 of the Manual of Patent Examining Procedure, prosecution in the above-referenced patent application has been reopened through a Request for Continued Examination and the appeal pending before the Board of Patent Appeals and Interferences in the above-referenced patent application has been concurrently withdrawn, prior to a decision by the Board.

Applicant has chosen to reopen prosecution because Examiner made arguments that may be relevant to this application in a related application, application number 09/902,912, titled Gate Array Architecture, also to Possley. By the amendments and remarks provided herein, Applicant has addressed all outstanding issues presented in Examiner's Final Office Action and in Examiner's Answer to Applicant's Appeal Brief.

This application has been reviewed in light of the Final Office Action, mailed March 7, 2001, and in light of Examiner's Answer to Applicant's Appeal Brief, mailed May 24, 2002 (hereinafter "Examiner's Answer"). Claims 1-11, 21-26 and 44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tran, et al. (US-5,780,883) (hereinafter "Tran") in view of Sato (US-4,611,236). Reconsideration of the above-referenced patent application in view of the amendments and remarks provided herein is respectfully requested.

Claims 1-11, 21-26 and 44 are pending in the application. Claims 1, 4, 5, 21, and 23-26 are currently amended. Claims 24-26 have been broadened. Claim 12 was cancelled earlier and was later reinstated as claim 44. Claims 13-20 were withdrawn earlier and are being prosecuted in a separate continuation patent application. Claims 27-43 were cancelled earlier and are being

prosecuted in a separate continuation patent application. No claimed subject matter of any kind has been surrendered by these actions.

A minor omission is noted in the specification. This minor omission was made inadvertently and without deceptive intent. Appropriate corrections have been made by the foregoing amendments. It is respectfully requested that Examiner approve and enter these minor corrections.

I. REJECTIONS OF CLAIMS

Examiner, under section 103 of the patent statute, has rejected claims 1-11, 21-26, and 44. It is well established that for a *prima facie* rejection under section 103, Examiner must provide a prior art document or set of documents that, in combination, have each and every limitation of the rejected claims. See, for example, the Manual of Patent Examining Procedure (hereinafter "MPEP") section 2143 ("To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.") This, of course, is to be distinguished from anticipation, where each and every limitation must be shown within a single document. It is asserted that Examiner has failed to establish a *prima facie* case.

Examiner has stated that Applicant is wrong in his construction of the claims. Specifically, Examiner states, on, for example, page 6 of Examiner's Answer: "'[O]ne' in claim 1 and 21 refers to 'polysilicon gate', not 'one of the regions forms both N-type and P-type transistors'." Suffice it to say that Appellant believes Examiner is correct and that Applicant's previous position on this issue is mistaken. Nonetheless, Examiner has still failed to present a *prima facie* case under the construction

that Examiner advocates. Specifically, neither Tran nor Sato, either separately or in combination, teaches, shows, or even suggests at least one polysilicon landing site forming N-type and P-type transistors.

A. The Combination of Sato and Tran.

Examiner has stated, on page 3 of Examiner's Answer, that "Sato discloses in figure 9 that one gate can be formed on both N-type and P-type transistors to form the basic cells. Therefore, it would have been obvious to one of ordinary skill in the art to form a single polysilicon gate in Tran on both N-type and P-type transistors to form a basic cell as taught by Sato." However, Examiner is clearly reaching. Sato, by itself, does not even teach, suggest, or describe forming a single polysilicon gate to connect N-type and P-type transistors. Therefore, to say that based on Sato it would have been obvious to modify Tran to do so is misplaced. It is clear that this limitation as now recited in, for example, claim 1 and as correctly interpreted, is not present in any of the cited patents, either individually or in combination.

Examiner, on page 5 of Examiner's Answer, also responds to Applicant's argument that Tran is deficient in that it would require additional layers of metallization, in contrast to the subject matter of the rejected claims. Examiner states: "Since the gate electrodes are formed in advance over the N-type and P-type transistors as showed [sic] in figure 9, there is no need to form additional layers of metallization to connect N-type and P-type transistors as argued." Examiner could not be more incorrect in this regard. It is precisely because the cell layout is determined "in advance" that the additional layers would be required in Tran. This is because in these designs a single cell approach is being used to meet the requirements of a variety of customers without knowing, at the time the single cell is designed, what the specifics of the design for each customer will ultimately be. In Tran, because the N-type and P-type transistors are not coupled or connected, if a customer desires that they be connected or coupled this will involve additional layers of metallization. Thus, the subject

matter of the rejected claims provides several advantages over Tran, including reducing the number of layers of metallization.

B. Motivation to Combine Patents.

In addition to failing to meet the limitations of the rejected claims, the combination proposed by Examiner is improper. Examiner responds to this argument on page 6 of Examiner's Answer. Examiner states: "The teaching in Tran is not limited to a mulitplexer circuit and the teaching in Sato is not limited to a RAM cell." However, this response misses the point.

Even granting, simply for the sake of argument, that Examiner's statement is correct, Examiner's point is still legally insufficient to establish a motivation to combine. Even if Examiner is correct that these disclosures, by their own terms, do not necessarily limit themselves, Examiner fails to address the fact that, based on the contents of these disclosures, one of ordinary skill would not attempt the combination Examiner proposed. If they are unlimited, as he indicates, this still does not provide the missing motivation or suggestion to combine that is required.

This type of reasoning is precisely what the Federal Circuit has warned against. For example, in *In re Rouffet* the Federal Circuit stated:

> In this case, the Board . . . relied upon the high level of skill in the art to provide the necessary motivation. The Board did not, however, explain what specific understanding or technological principle within the knowledge of one of ordinary skill in the art would have suggested the combination. Instead, the Board merely invoked the high level of skill in the field. If such a rote invocation could suffice to supply a motivation to combine, the more sophisticated scientific fields would rarely, if ever, experience a patentable technical advance. Instead, in complex scientific fields, the Board would routinely identify the prior art elements in an application, invoke the lofty level of skill, and rest its case for rejection. To counter the potential weakness in the obviousness construction, the suggestion to combine requirement stands as a critical safeguard against hindsight analysis and rote application of the legal test for obviousness.

In re Rouffet, 47 USPQ2d 1453, 1458 (Fed. Cir. 1998) (emphasis added).

It is respectfully asserted that here Examiner has engaged in the same practice the Federal Circuit criticized.

Examiner has not provided any underlying principles or technical understanding that would motivate one of ordinary skill to make the combination and, instead, has merely engaged in "hand waving" to argue that, nonetheless, making the combination would be obvious to one of ordinary skill in the art anyway. As the Federal Circuit has indicated, this approach is improper.

C. Examiner's New Ground of Rejection in Examiner's Answer.

Examiner raised a new ground of rejection on page 4 of Examiner's Answer, stating "Claims 1-11, 21-26 and 44 are alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over Sato." Applicant points out that the same requirements for a *prima facie* case, as indicated above, apply in this instance. Here, Examiner has based the rejection on an individual patent rather that a combination of patents. Such a situation is even less likely to meet the appropriate legal burden on Examiner because, as stated in *In re Kotzab*, "Even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference." *In re Kotzab*, 54 USPQ2d 1308 (Fed. Cir. 2000).

Here, Examiner has failed to provide the appropriate motivation for such a modification. More to the point, Examiner does not even attempt to address the limitation of the rejected claims regarding at least one polysilicon landing forming both N-type and P-type transistors. Rather, Examiner states on page 4 of Examiner's Answer that "[I]t would have been obvious that Sato discloses a single gate electrode formed on two smaller N-type and P-type diffusions to form smaller N- and P-type transistors and another single gate electrode formed on two larger diffusions to form larger N- and P-type transistors." However, it is clear that this does not address what is recited in the

rejected claims, such as claim 1. Furthermore, by relying solely on Sato, the Examiner has failed to provide any prior art that would provide the basis to modify the teachings of Sato to meet the limitations of the rejected claims.

II. CURRENT AMENDMENTS TO CLAIMS

Having respectfully traversed all of Examiner's rejections of the claims pending in this application, Applicant nevertheless offers and respectfully requests that Examiner enter the currently amended claims. Applicant respectfully asserts that the claims in this application are in condition for allowance without the current amendments and, as such, respectfully reserves the right to pursue the original claim language on any subsequent appeal. Yet, the current amendments further clarify and distinguish the claims. Therefore, in the interests of advancing prosecution and putting the claims in this application in condition for allowance, Applicant offers the current amendments to the claims.

Claim 1 now specifically recites:

> An integrated circuit comprising: a gate array architecture;
>
> said gate array architecture including a semiconductor substrate having a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites, at least one forming N-type and P-type transistors;
>
> wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors; and
>
> wherein said transistors are formed in said gate array architecture so that an interconnect disposed thereon is capable of connecting said smaller transistors to form internal clock buffers.

Applicant respectfully asserts that this amendment further distinguishes claim 1 from the cited patents in at least the respect that Tran teaches that larger transistors are used for inverters and logic gates and Sato requires large transistors to implement inverters. Therefore, it is respectfully requested that Examiner withdraw all rejections of claim 1 and enter the amended claim.

Claims 2-11 and 44 dep nd from claim 1 and incorporate all the limitations thereof. Since the current amendment to claim 1 further distinguishes it from the cited patents, claims 2-11 and 44 are likewise further distinguished from the cited patents. Therefore, it is respectfully requested that Examiner withdraw all rejections of claims 2-11 and 44 and enter the amended claims.

Claim 21 is currently amended in a fashion like the currently amended claim 1. As with claim 1, Applicant respectfully asserts that this current amendment to claim 21 further distinguishes claim 21 from the cited patents in at least the respect that Tran teaches that larger transistors are used for inverters and logic gates and Sato requires large transistors to implement inverters. Therefore, it is respectfully requested that Examiner withdraw all rejections of claim 21 and enter the amended claim.

Claims 22-26 depend from claim 21 and incorporate all the limitations thereof. Since the current amendment to claim 21 further distinguishes it from the cited patents, claims 22-26 are likewise further distinguished from the cited patents. Therefore, it is respectfully requested that Examiner withdraw all rejections of claims 22-26 and enter the amended claims.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application are in condition for allowance. Reconsideration of this patent application and early allowance of all the claims is respectfully requested. If Examiner has any questions, they can be addressed to the undersigned at (503) 712-1565 or to Howard Skaist at (503) 264-0967.

Respectfully submitted.

Jay Beale

Attorney Docket: 042390.P6643

Patent Agent
Reg. No. 50,901

Dated: 11 April, 2003

c/o Blakely, Sokoloff, Taylor & Zafman, LLP
12400 Wilshire Blvd., Seventh Floor
Los Angeles, CA 90025-1026
(503) 264-0967

***I hereby certify** that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner of Patents, Washington, D.C. 20231 on:*

April 14 2003
Date of Deposit

Angie C. Farr
Name of Person Mailing Correspondence

Angie C. Farr 4.14.03
Signature *Date*